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BLF20M10LS200P, 1975-2025 MHz

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Application Report

Document information

Status	General Publication
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Abstract	Measurement results of 1975-2025 MHz amplifier with the BLF20M10LS200P

1. Revision History

Table 1: Report revisions

Revision	Date	Description	Author
1.0	2026-01-29	Initial document	Naser H.R Miveroud

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5. Description

This report presents measurement results of Ampleon's 2.0GHz 200W LDMOS amplifier. The device used is BLF20M10LS200P, Ampleon's 10th generation 32V LDMOS transistor in high performance air cavity package. The presented demo is operating at full 1.975-2.025 GHz ISM band. The results are presented for a typical application. However, the demo can be tuned for different efficiency/power tradeoffs.

For further details and conditions, customers can contact an Ampleon marketing/sales representative.

Table 2: Mechanical characteristics

Parameter	Description	Unit
L x W	60 x 30	mm
PCB assembly height	4	mm

Table 3: Board Specifications

Parameter	Value
Manufacturer	Rogers
Type	TC350
Dk	3.5 @ 10GHz
Df	0.0037 @ 10GHz
Total PCB thickness	0.508 mm (20mil)
Copper thickness	35um (1 oz)
Board dimensions	60 x 30 mm

6. Demo Board

Figure 1 illustrates the demo board's top view. The transistor and PCB are soldered to copper baseplate and mounted on a water-cooled heatsink for measurement.

The demo board has a very compact size of 6cm x 3cm only.

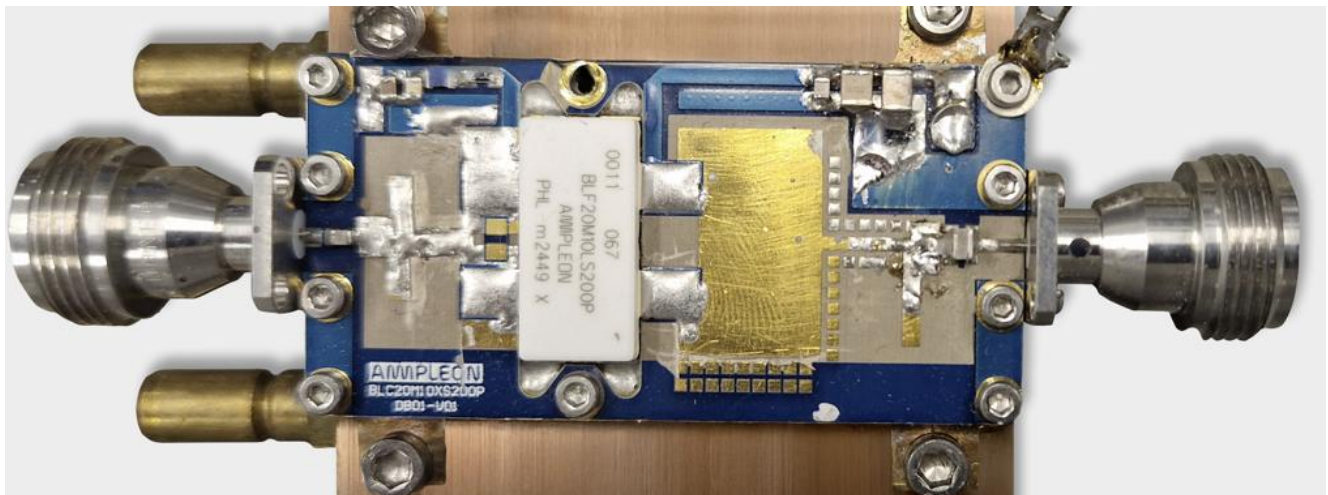


Figure 1 Demo top view

Table 4 summarizes the key parameters of the demo. Output power is more than 200W in CW mode. Measurement is done at the output connector (RF OUT) of the demo.

Tables 5 and 6, and Figures 3 to 8 depict detailed values of the measurement for the demo.

Table 4: General Specifications, $T_{\text{base plate}} = 25^{\circ}\text{C}$

Symbol	Parameter	Unit	Min	Typ	Max
F	Frequency of operation	MHz	1975	-	2025
V_{DD}	Drain voltage of LDMOS transistor	V	-	-	32
I_{DD}	Current consumption of LDMOS transistor	mA	-	9.5	-
P_{OUT}	Output power ¹	W	-	200	-
η_{DRAIN}	Drain efficiency ²	%	-	68	-
P_{DISS}	Dissipated power	W	-	100	-
H	Level of harmonics	dBc	-	-	- 40

¹ Typical output power of 200W is achieved with $V_{\text{DD}} = 32\text{V}$ at 2dB compression point ($P_{2\text{dB}}$).

² Typical efficiency of 68% is achieved with $V_{\text{DD}} = 32\text{V}$ at 2dB compression point ($P_{2\text{dB}}$).

6.1 RF characteristics

Test signal: CW ; VDD = 30.8V, Idq = 5mA; T_{base_plate} = 25°C.

Table 5: RF characteristics in CW mode, VDD = 30.8V, Idq = 5mA

Freq (MHz)	Gmax (dB)	P1dB (W)	P3dB (W)	Eff_P1dB (%)	Eff_P3dB (%)	Eff_max (%)	Pout @ Eff_max (W)
1975	18.4	195	216	68.4	67.5	68.4	200
2000	18.7	187	210	68.1	67.2	68.1	192
2025	18.6	182	207	68.5	67.6	68.6	186

Test signal: CW; VDD = 32V, Idq = 5mA; T_{base_plate} = 25°C.

Table 6: RF characteristics in CW mode, VDD = 32V, Idq = 5mA

Freq (MHz)	Gmax (dB)	P1dB (W)	P3dB (W)	Eff_P1dB (%)	Eff_P3dB (%)	Eff_max (%)	Pout @ Eff_max (W)
1975	18.6	206	227	66.9	65.1	66.9	203
2000	18.9	199	222	67.0	65.6	67.0	200
2025	18.8	194	219	67.6	66.5	67.7	198

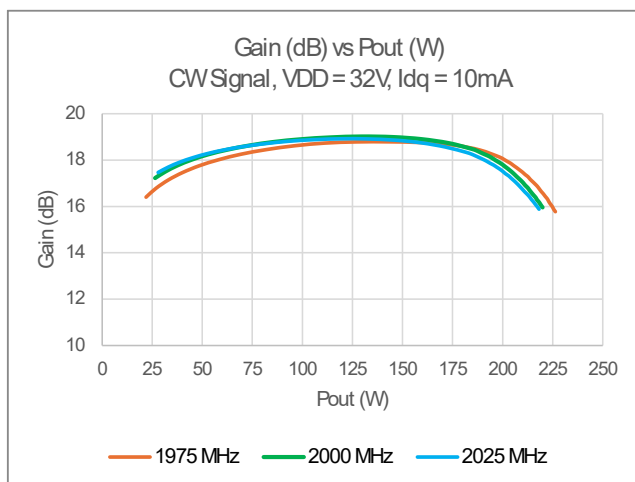


Figure 2 Gain (dB) over output power (W),
CW signal, VDD = 32V, Idq = 10mA

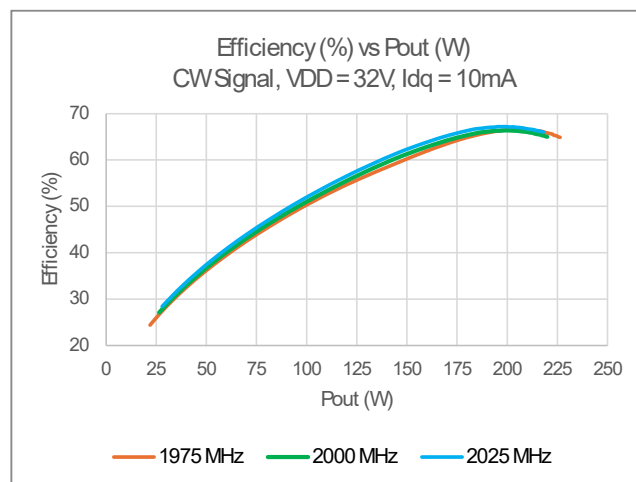


Figure 3 Efficiency (%) over output power (W),
CW signal, VDD = 32V, Idq = 10mA

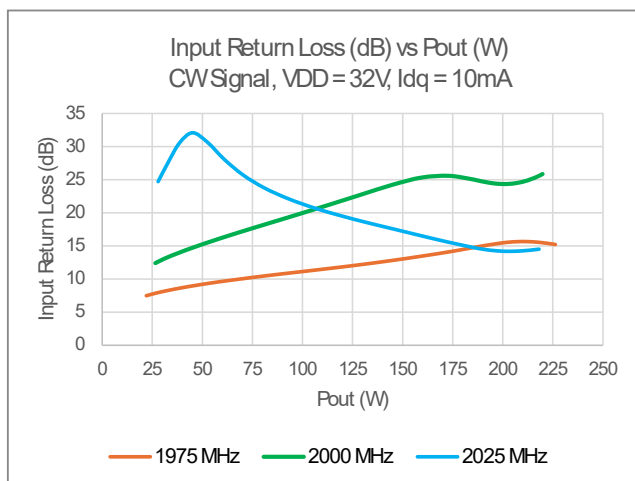


Figure 4 Return Loss (dB) over output power (W),
CW signal, VDD = 32V, Idq = 10mA

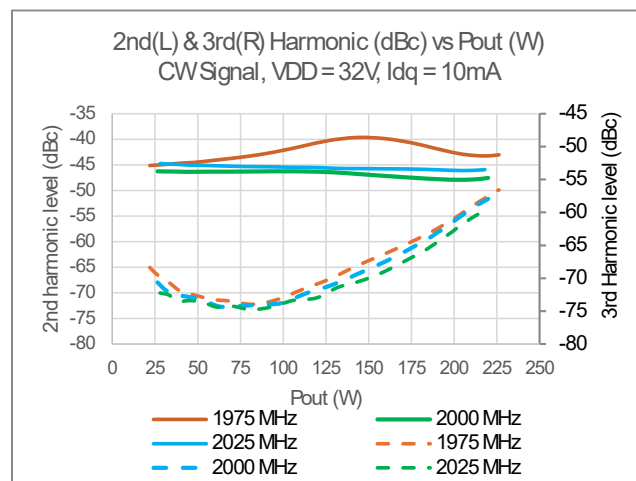


Figure 5 Harmonic level (dBc) over output power (W),
CW signal, VDD = 32V, Idq = 10mA

6.2 Thermal characteristics

Figure 7 illustrates the IR image of the demo after reaching thermal equilibrium with water cooling. The maximum temperature in the demo is 66.6 °C. Measurements is done at $f = 2.0\text{GHz}$, and $P_{out} = 200\text{W}$ under CW signal while temperature of the baseplate kept at 30°C.

Transistor's drain leads and the output DC block capacitor covered with special black pain for accurate measurement of the temperature.

The test condition in which the IR image of Figure 7 is captured is as follows:

- CW Signal
- $V_{DD} = 32\text{V}$, $I_{dq} = 10\text{mA}$
- $P_{out} = 200\text{ W}$
- Efficiency = 65 %
-

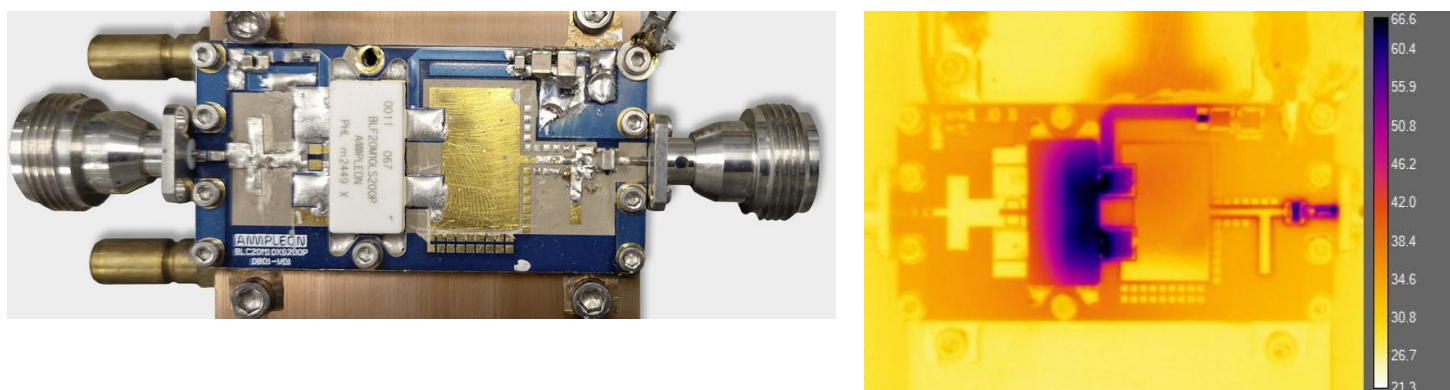


Figure 7 IR image of the demo after reaching thermal equilibrium and operating at $P_{out} = 200\text{W}$, $V_{DD} = 32\text{V}$, $T_{base_plate} = 30^\circ\text{C}$

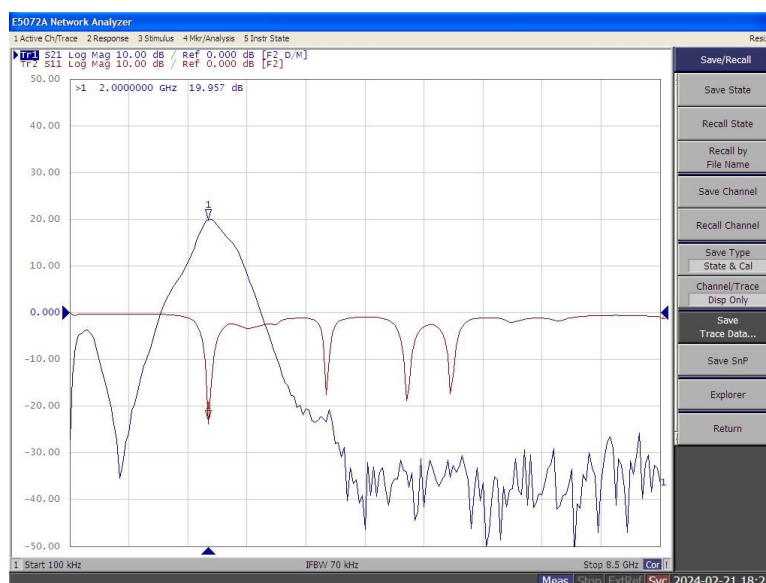


Figure 6 Input return loss dB) and Gain (dB) at $P_{in} = 0\text{dBm}$, $V_{DD} = 32\text{V}$, $I_{dq} = 1\text{A}$

7. Bill of materials

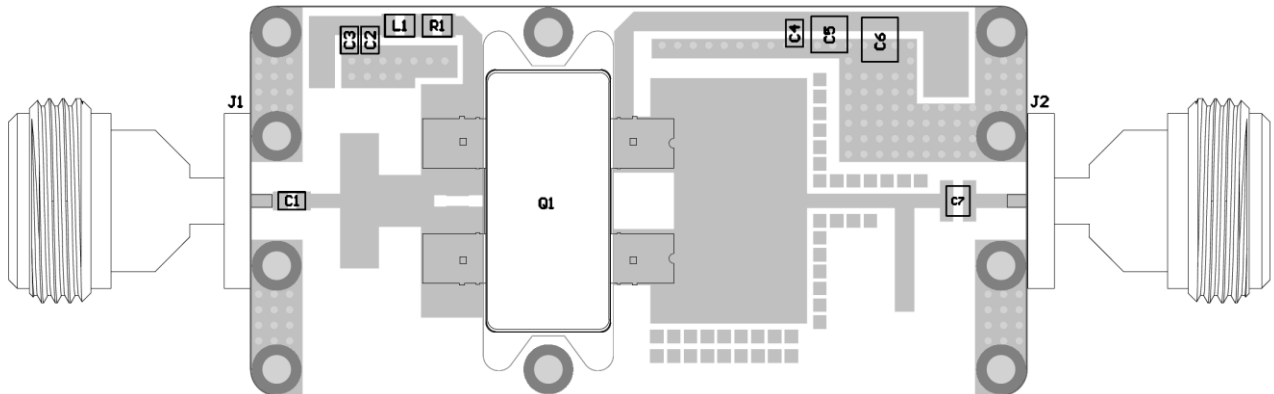


Figure 19 PCB layout and component assembly

Table 7: Bill of Materials

Designator	Group	Value	Tolerance	Name	Manufacturer	Quantity
C1	Capacitor	33pF	±5%	ATC600F330JW250XT	ATC	1
C2, C4	Capacitor	100pF	±5%	ATC600F101JW250XT	ATC	2
C3	Capacitor	4.7uF		0805 X7R	Murata	1
C5	Capacitor	1000pF	±5%	ATC800B102JW50XT	ATC	1
C6	Capacitor	10uF	±10%	C3225X7R2A106K	TDK	1
C7	Capacitor	33pF	±5%	ATC800R330BW500T	ATC	1
L1	Inductor	12nH	±2%	0805HP-12NXGRC	Coilcraft	1
Q1	LDMOS Transistor			BLF20M10LS200P	Ampleon	1
PCB Material TC350, 20mil with Type II vias						

7. Abbreviations

Table 8: Abbreviations

Parameter	Description
F	Frequency
CW	Continuous Wave
G_{max}	Maximum Gain
P_{1dB}	1 dB Compression Point of the Gain
V_{DD}	Drain Voltage
V_{GS}	Gate Voltage
η_{DRAIN}	Drain Efficiency
GaN	Gallium Nitride

VSWR	Voltage Standing Wave Ratio
δ	Duty Cycle
t_p	Pulse Width
RF	Radio Frequency
P_L	Power Delivered to 50 Ω Load at RF OUT Connector
S21	Small Signal Gain (S-parameter measurement in 50 Ω System)
Pin	Input Power to the Amplifier at RF IN Connector
Pout	Output Power of Amplifier at RF OUT Connector

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